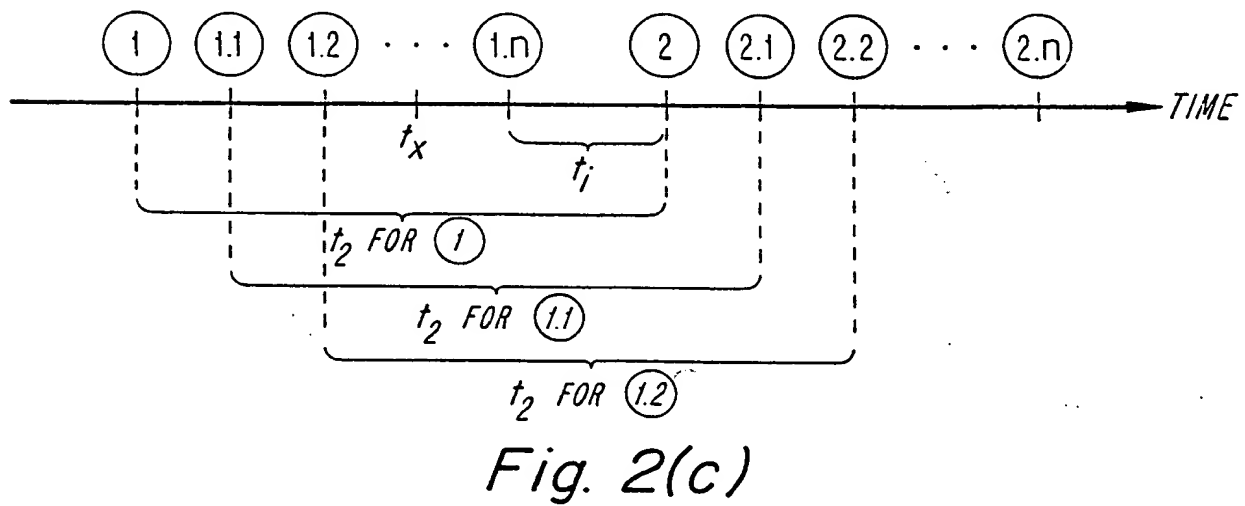
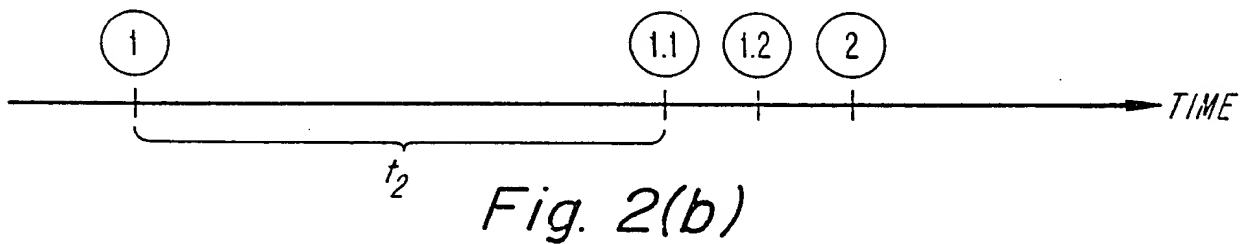
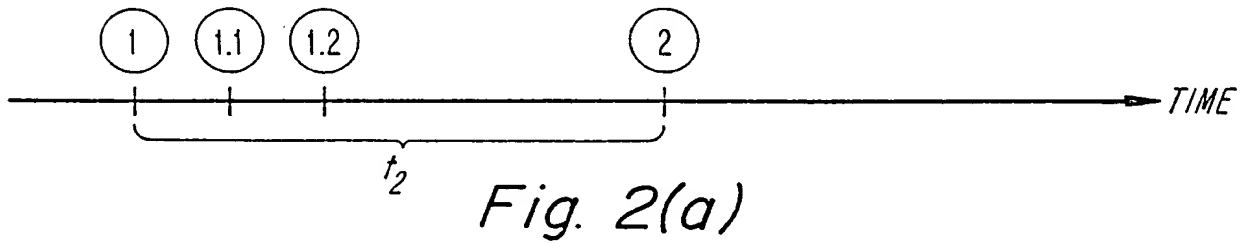
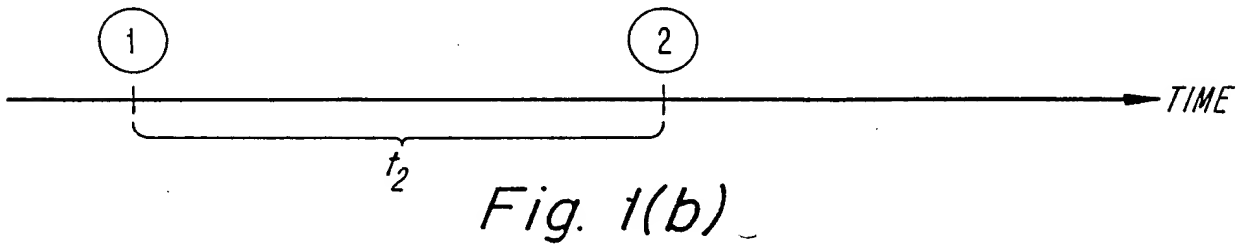
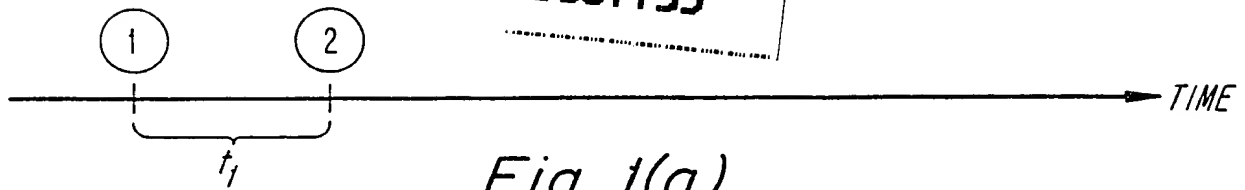
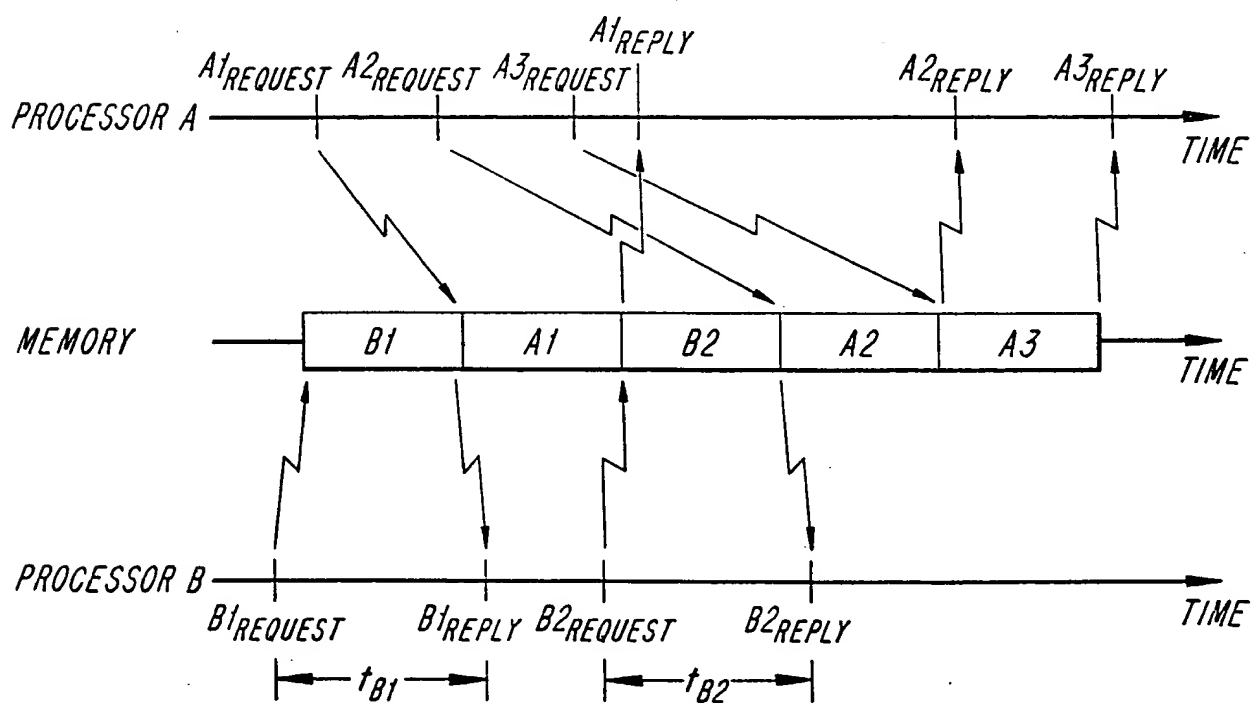
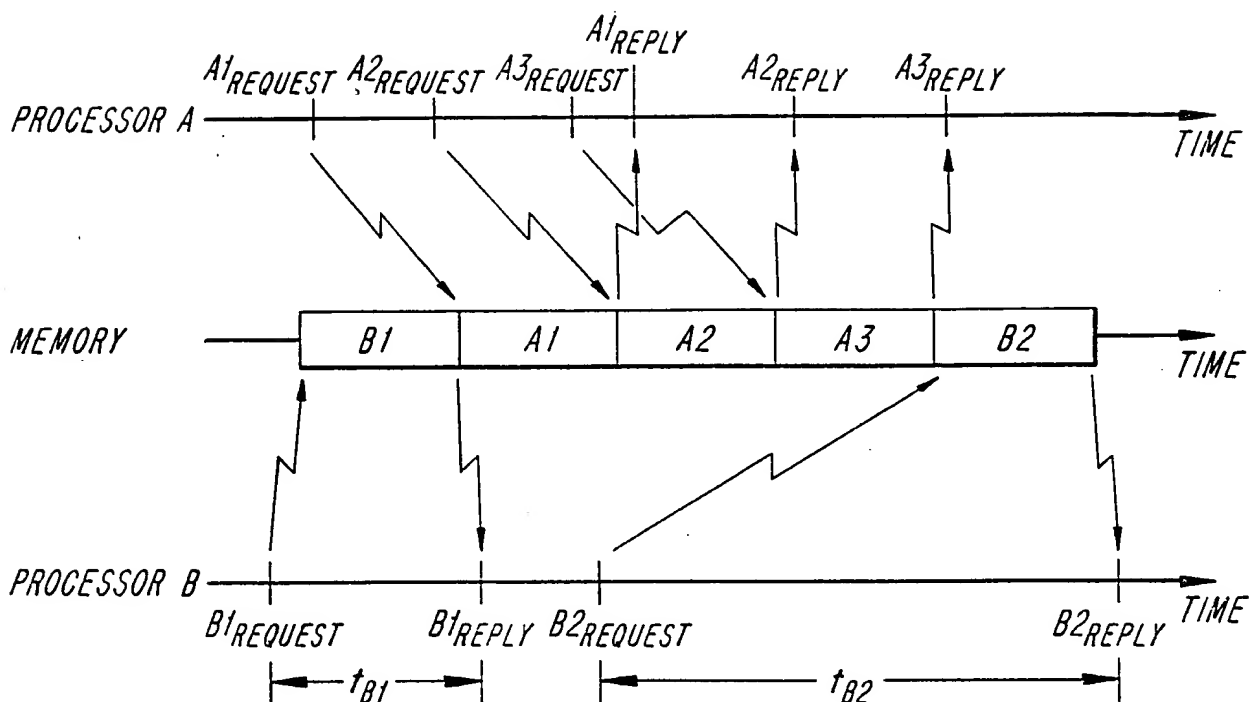


5867735



# THE UNIVERSITY OF CHICAGO



The diagram illustrates a system architecture with the following components and connections:

- Cache (20):** A rectangular block on the left side of the diagram.
- Processors (30<sub>0</sub>, 30<sub>1</sub>, ..., 30<sub>m</sub>):** A vertical column of rectangular blocks in the center.
- Non-Blocking Load Buffer (10):** A rectangular block located between the Cache and the Processors.
- Devices (50<sub>0</sub>, 50<sub>1</sub>, ..., 50<sub>n</sub>):** A vertical column of rectangular blocks on the right side of the diagram.

**Connections:**

- A horizontal bus line (40) runs across the middle of the diagram, passing through the Non-Blocking Load Buffer (10).
- Cache to Buffer:** A downward arrow (41) connects the Cache (20) to the Non-Blocking Load Buffer (10).
- Buffer to Cache:** An upward arrow (42) connects the Non-Blocking Load Buffer (10) to the Cache (20).
- Buffer to Processors:** Downward arrows connect the Non-Blocking Load Buffer (10) to each of the Processors (30<sub>0</sub>, 30<sub>1</sub>, ..., 30<sub>m</sub>).
- Processors to Buffer:** Upward arrows connect each of the Processors (30<sub>0</sub>, 30<sub>1</sub>, ..., 30<sub>m</sub>) to the Non-Blocking Load Buffer (10).
- Processors to Devices:** Downward arrows connect each of the Processors (30<sub>0</sub>, 30<sub>1</sub>, ..., 30<sub>m</sub>) to the corresponding Device (50<sub>0</sub>, 50<sub>1</sub>, ..., 50<sub>n</sub>).
- Devices to Buffer:** Upward arrows (61) connect each of the Devices (50<sub>0</sub>, 50<sub>1</sub>, ..., 50<sub>n</sub>) to the Non-Blocking Load Buffer (10).
- Buffer to Devices:** Downward arrows (60) connect the Non-Blocking Load Buffer (10) to each of the Devices (50<sub>0</sub>, 50<sub>1</sub>, ..., 50<sub>n</sub>).
- Device to Ready:** Each Device (50<sub>i</sub>) has a "READY" output line that leads to a corresponding "READY" input line on the Non-Blocking Load Buffer (10).

APPROVED	C.G. FIG. 3(6)	
	CLASS	SUBCLASS
BY	395	872
DRAFTSMAN		

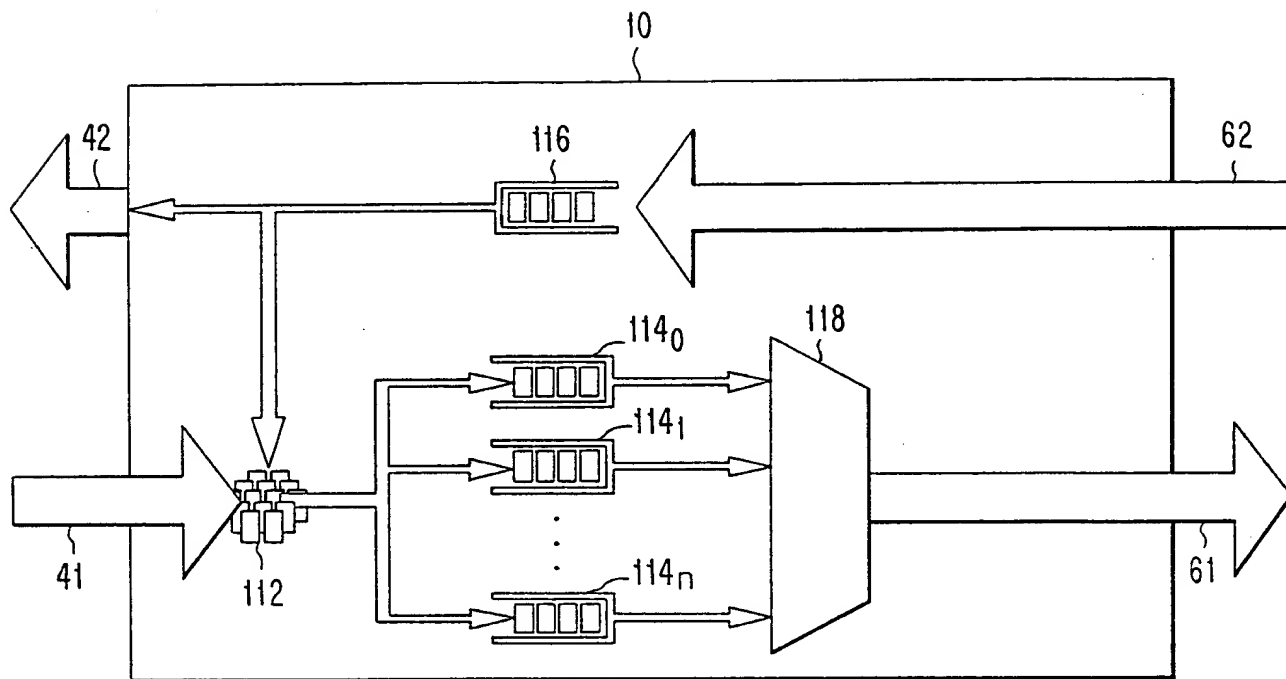


Fig. 5

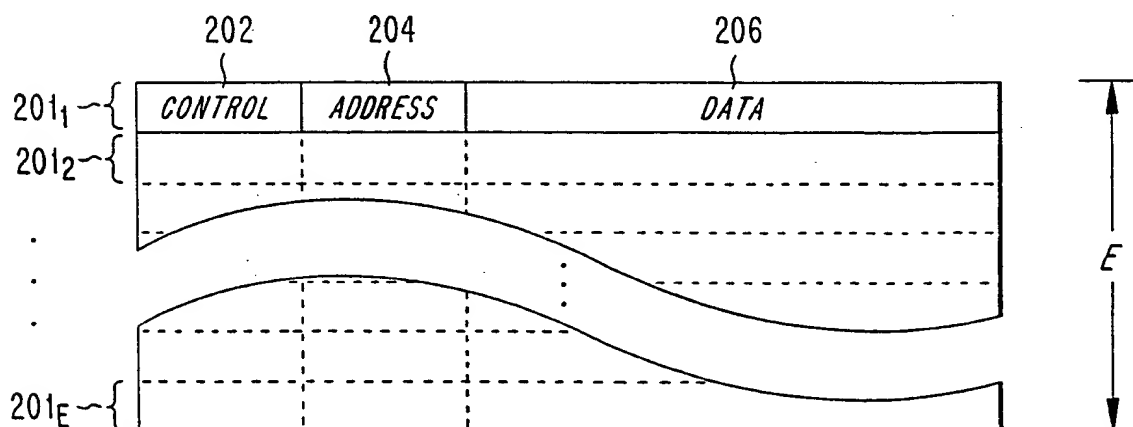


Fig. 6

200

APPROVED	O.G. FIG. 3(2)	
BY	CLASS	SUBCLASS
DRAFTSMAN	395	872

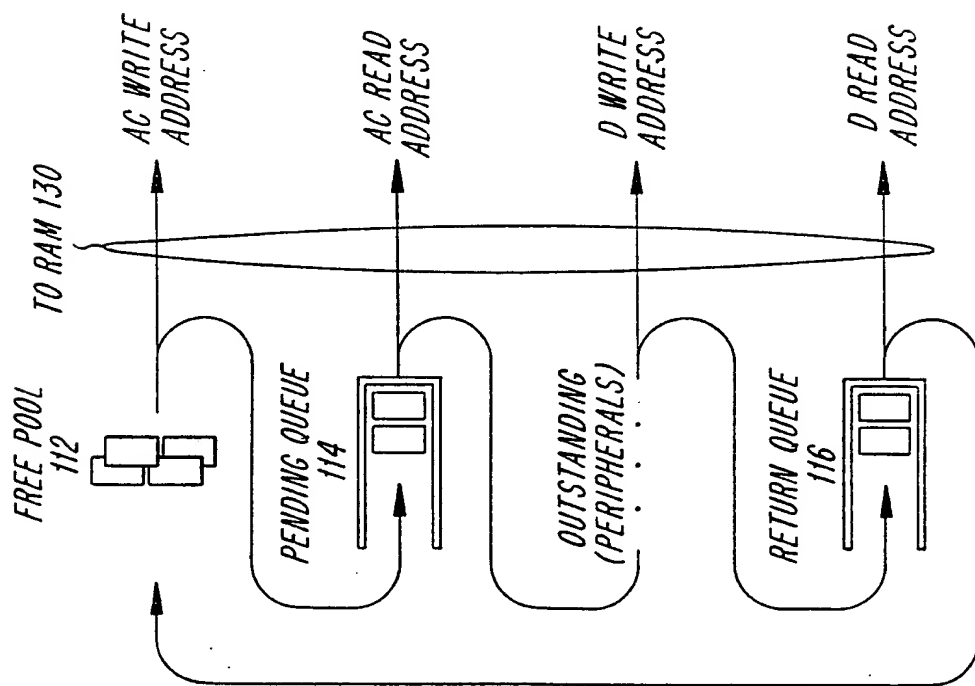


Fig. 7(a)

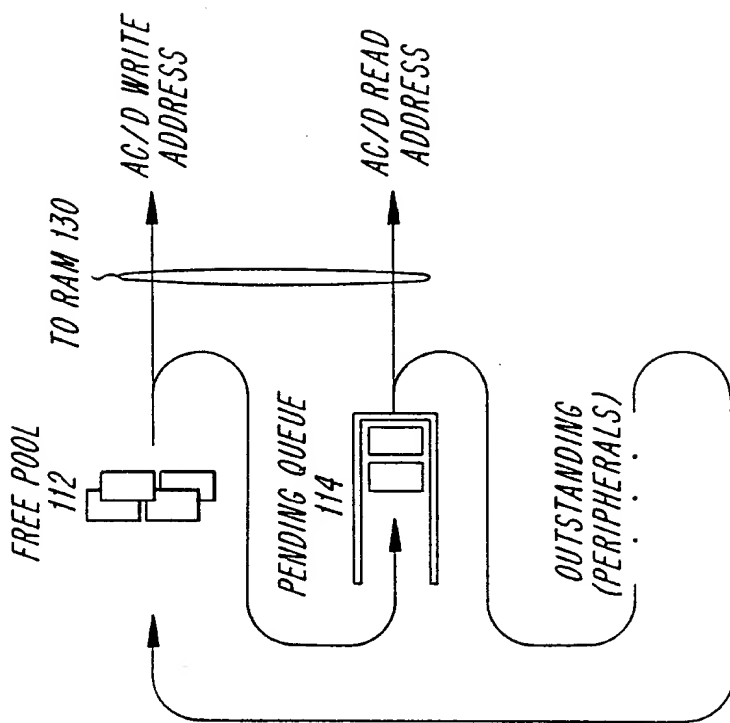


Fig. 7(b)

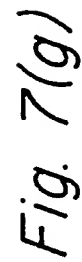


Fig. 7(f)

Fig. 7(e)

Fig. 7(d)

Fig. 7(c)

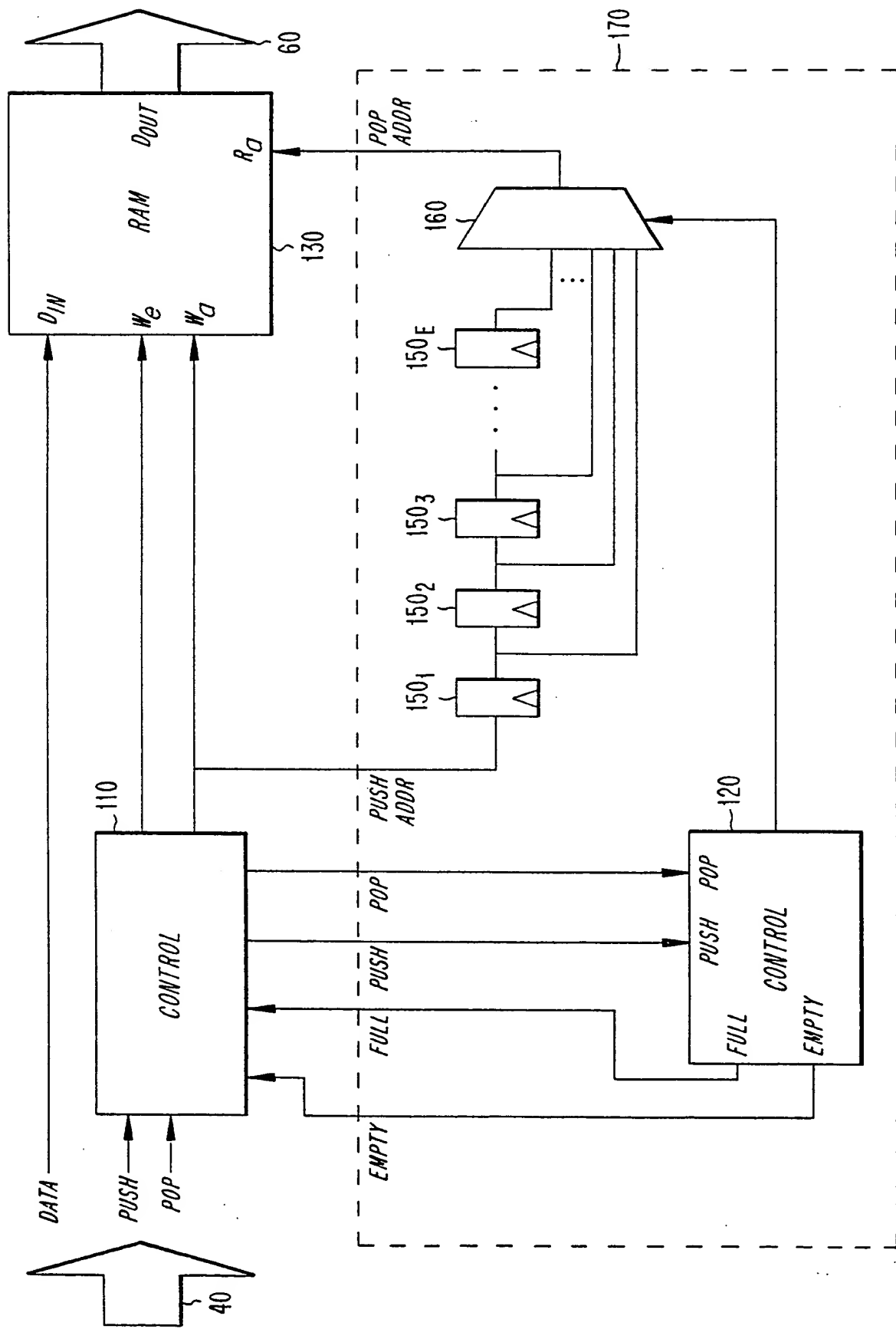


Fig. 8

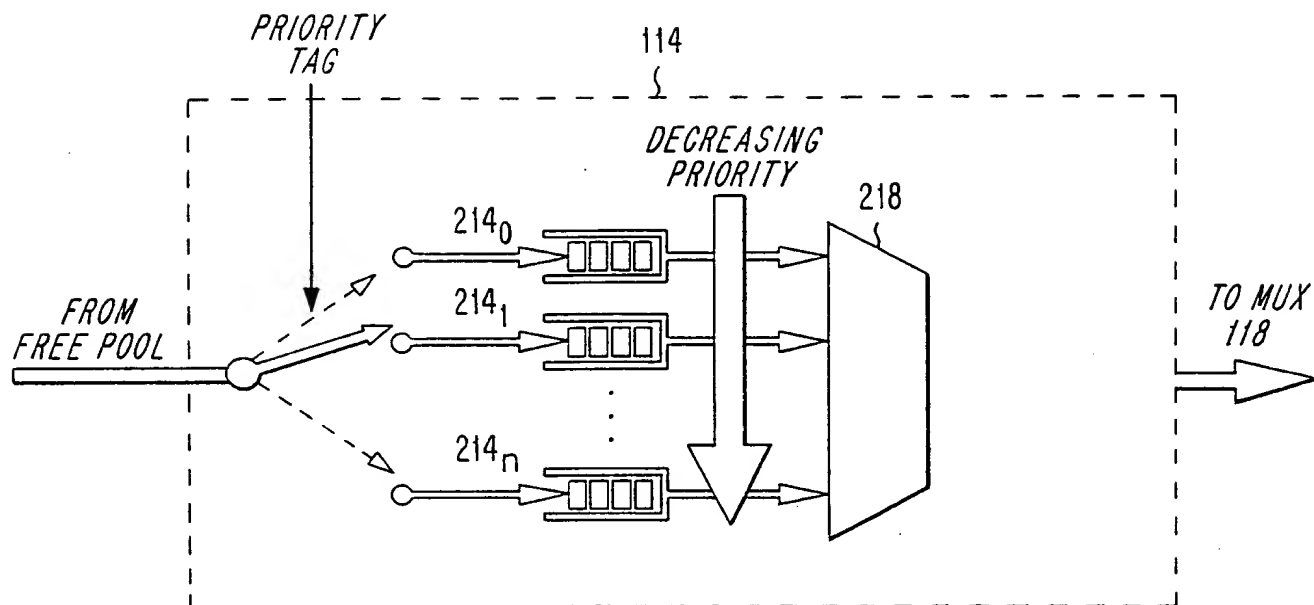


Fig. 9(a)

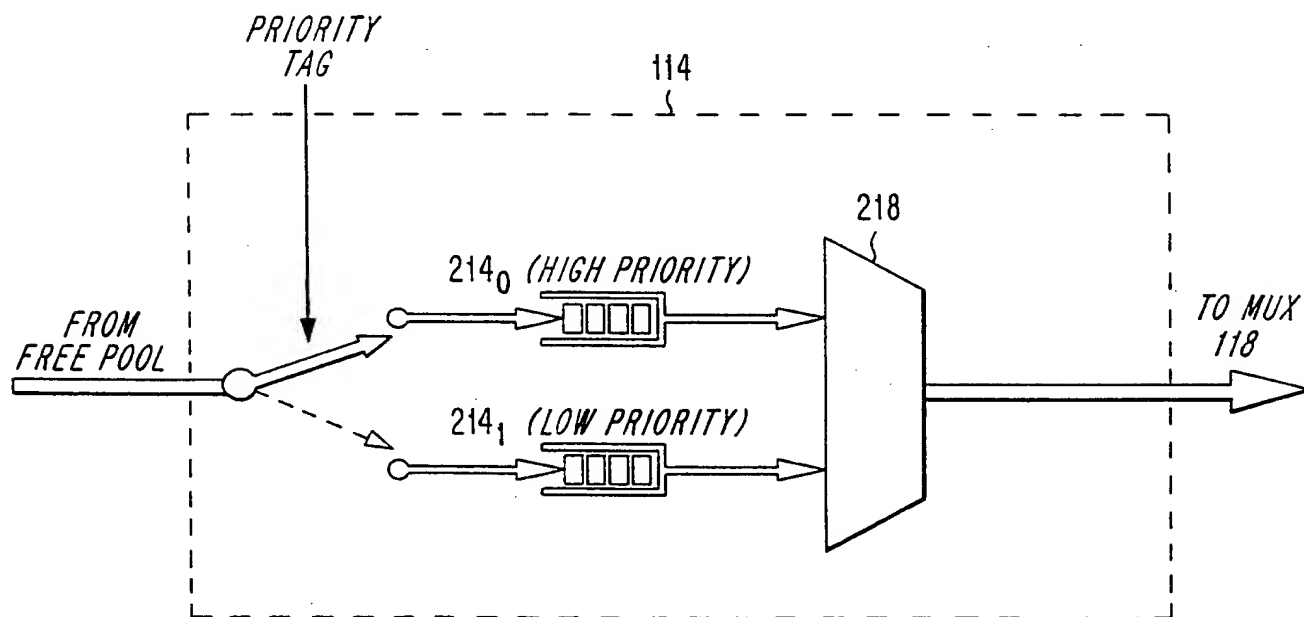


Fig. 9(b)



66000-6000000

APPROVED O.G. FIG. 3(6)  
 BY CLASS SUBCLASS  
 375 872  
 DRAFTSMAN

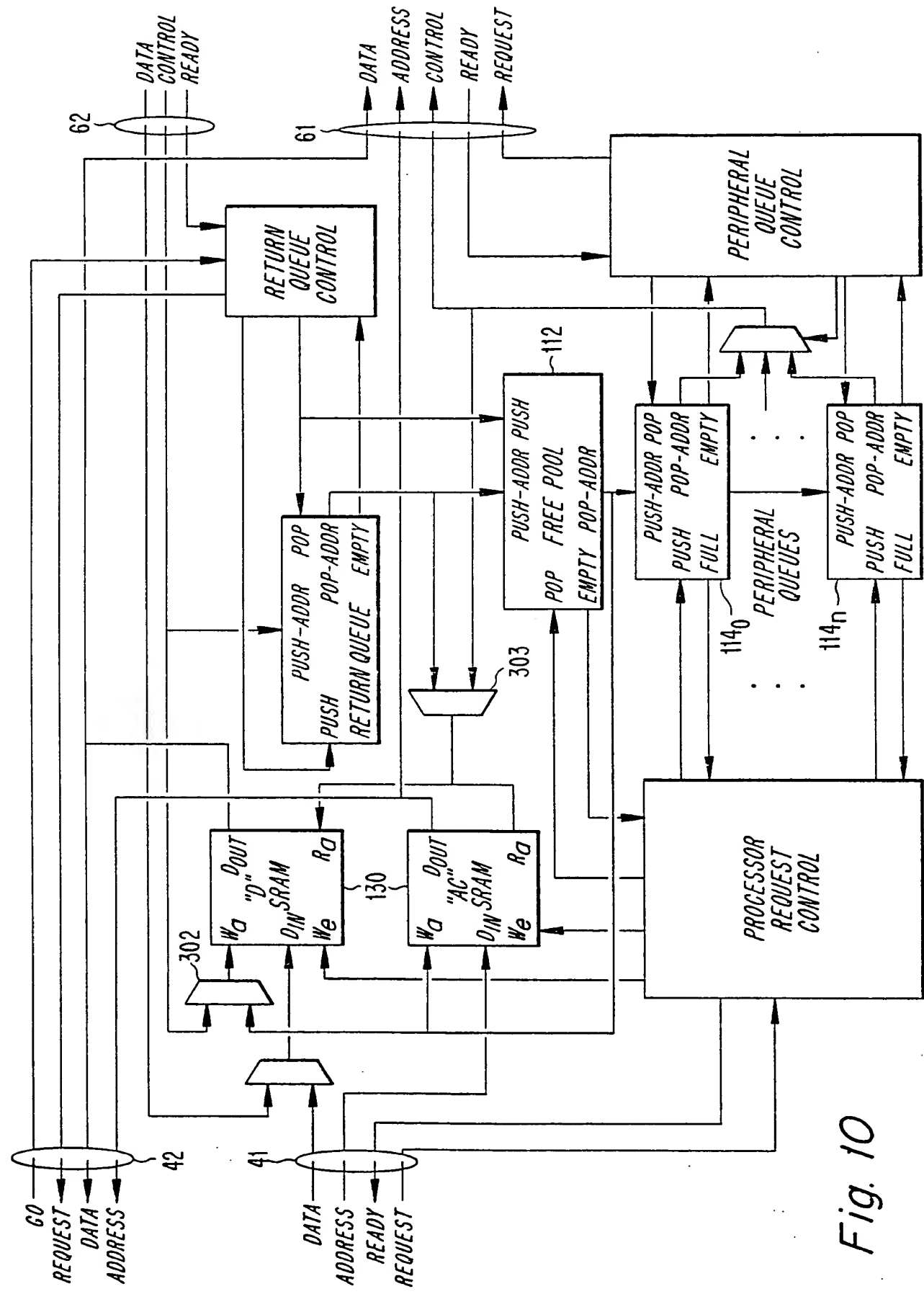


Fig. 10

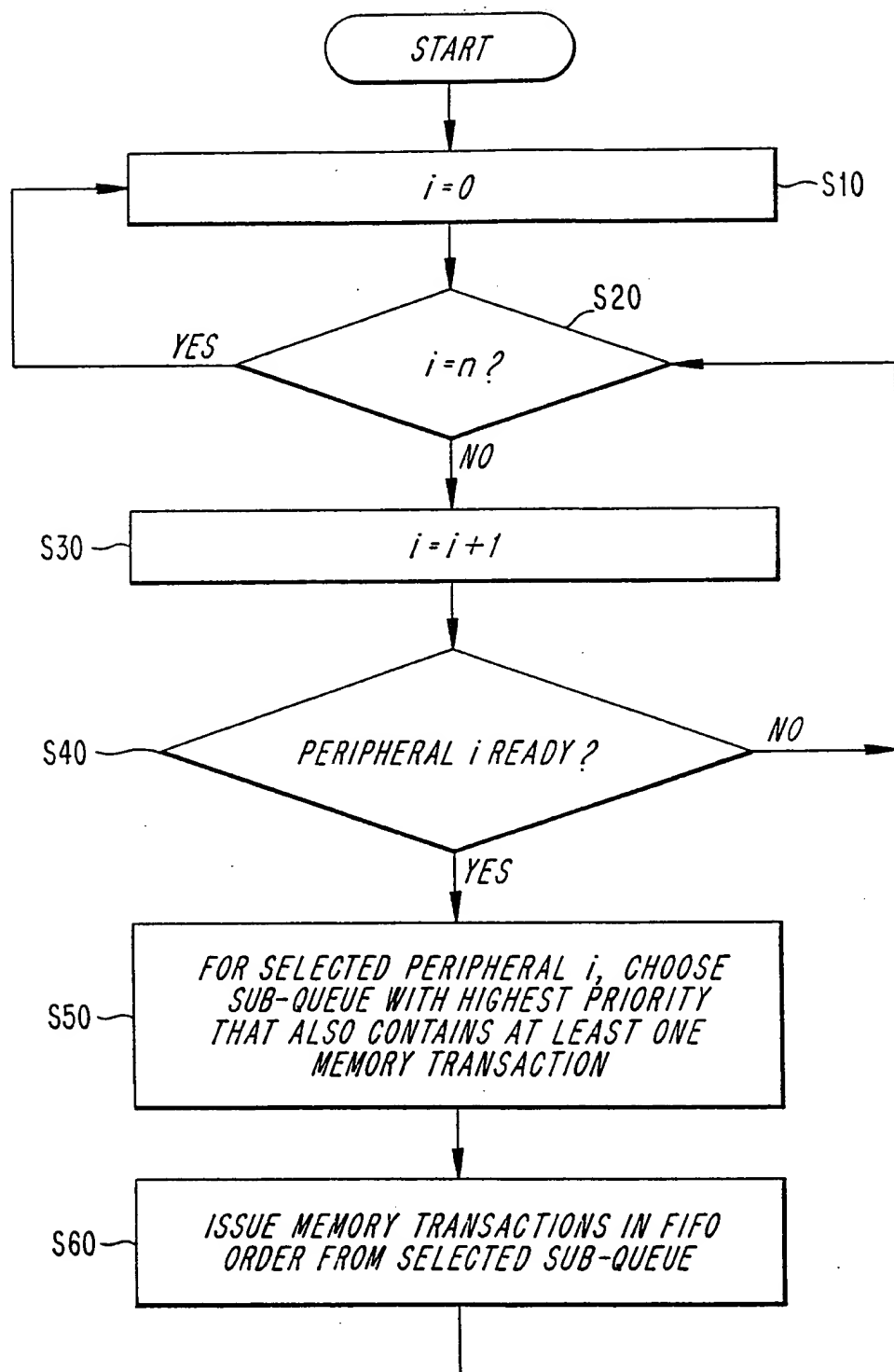


Fig. 11